Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the above-captioned application.

1. (Currently amended): A method for fabricating a structure in the form of a plate comprising at least one substrate ~~(2)~~, a superstrate ~~(3)~~ and at least one intermediate layer ~~(4)~~ interposed between the substrate and the superstrate, ~~characterized in that it consists in~~ the method comprising selecting an intermediate layer ~~(4)~~ comprising at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material, and applying a heat treatment to said structure ~~(1)~~ so that, in the temperature range of said heat treatment, the intermediate layer is plastically deformable and the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities ~~(7)~~ in the intermediate layer.

2. (Currently amended): The method as claimed in claim 1, ~~characterized in that~~ wherein the heat treatment produces micro-bubbles or micro-cavities which weaken said intermediate layer.

3. (Currently amended): The method as claimed in claim 1, ~~characterized in that~~ wherein the heat treatment produces a rupture of said intermediate layer and, as a result, separation of the substrate and the superstrate.

4. (Currently amended): ~~A method for separating the substrate and superstrate in the structure obtained by the method as claimed in any one of the preceding claims, characterized in that it consists in~~ The method of claim 1, further comprising applying forces between the substrate ~~(2)~~

and the superstrate ~~(3)~~ to bring about the rupture of the intermediate layer between the substrate and the superstrate due to the presence of said micro-bubbles or micro-cavities.

5. (Currently amended): ~~A method for separating the substrate and superstrate in the structure obtained by the method as claimed in any one of claims 1 to 3, characterized in that it consists~~ ~~in~~in the method of claim 1, further comprising chemically attacking the intermediate layer ~~(4)~~ of the structure to at least partially remove said intermediate layer between the substrate and the superstrate.

6. (Currently amended): ~~The method as claimed in any one of the preceding claims, characterized in that the~~ The method of claim 1, wherein the substrate ~~(2)~~ and the superstrate ~~(3)~~ are formed from monocrystalline silicon and the intermediate layer ~~(4)~~ is formed from doped silica.

7. (Currently amended): A method for fabricating silicon wafers, ~~characterized in that it consists~~ ~~in~~comprising:

producing a structure ~~(1)~~ in the form of a plate comprising a substrate ~~(2)~~ formed from silicon, a superstrate ~~(3)~~ formed from silicon and a dielectric intermediate layer ~~(4)~~ comprising at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material;

then applying a heat treatment to said structure so that, in the temperature range of the heat treatment, the intermediate layer is plastically deformable and so that the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities ~~(7)~~ in the intermediate layer ~~(4)~~.

8. (Currently amended): The method as claimed in claim 7, ~~characterized in that~~ wherein the base material is formed from silica and the extrinsic atoms are atoms of phosphorus or boron,

thus forming an intermediate layer of phospho-silicate glass (P.S.G.) or boro-phospho-silicate glass (B.P.S.G.).

9. (Currently amended): The method as claimed in claim 8, ~~characterized in that~~ wherein the concentration of phosphorus is in the range from 6% to 14%.

10. (Currently amended): The method as claimed in claim 8, ~~characterized in that~~ wherein the concentration of boron is in the range from 0% to 4%.

11. (Currently amended): The method as claimed in ~~any one of claims 7 to 10, characterized in that~~ claim 7, wherein the heat treatment is carried out at a temperature in the range from 900°C to 1200°C.

12. (Currently amended): The method as claimed in ~~any one of claims 7 to 11, characterized in that it consists~~claim 7, wherein the method further comprises, prior to said heat treatment, ~~in~~ carrying out an operation for depositing said intermediate layer ~~(4)~~ on the substrate ~~(2)~~, or respectively the superstrate ~~(3)~~, and attaching the superstrate, or respectively the substrate, to said intermediate layer ~~(4)~~ by molecular wafer bonding.

13. (Currently amended): The method as claimed ~~in any one of claims 7 to 12, characterized in that~~in claim 7, wherein, on the intermediate layer ~~(4)~~ side, the substrate and the superstrate respectively comprise a thermal silicon oxide ~~(5, 6)~~.

14. (Currently amended): The method as claimed in ~~any one of claims 7 to 13, characterized in that it consists in~~ claim 7, further comprising exerting forces on said structure ~~(1)~~ in a manner such that rupture of said intermediate layer is brought about, resulting in separation of the

substrate and superstrate due to the presence of said micro-bubbles or micro-cavities ~~(7)~~ to obtain a wafer constituted by the substrate ~~(2)~~ and/or a wafer constituted by the superstrate ~~(3)~~.

15. (Currently amended): The method as claimed in ~~any one of claims 7 to 14, characterized in that it consists in~~ claim 7, further comprising chemically attacking said intermediate layer ~~(4)~~ of said structure ~~(1)~~ to bring about separation of the substrate and superstrate due to the presence of said micro-bubbles or micro-cavities to obtain a wafer constituted by the substrate ~~(2)~~ and/or a wafer constituted by the superstrate ~~(3)~~.

16. (Currently amended): The method as claimed in ~~any one of the preceding claims, characterized in that it consists in~~ claim 7, further comprising producing projecting portions ~~(8)~~ in the substrate ~~(2)~~ and/or the superstrate ~~(3)~~ on said intermediate layer ~~(4)~~ side.

17. (Currently amended): The method as claimed in ~~any one of the preceding claims, characterized in that~~ claim 16, wherein the projecting portions ~~(8)~~ are rectilinear and extend to the sides of the intermediate layer ~~(4)~~.

18. (Currently amended): The method as claimed in ~~any one of the preceding claims, characterized in that~~ claim 7, wherein at least some of said micro-bubbles or micro-cavities ~~(7)~~ are open-celled and at least some thereof constitute channels.

19. (Currently amended): The method as claimed in ~~any one of the preceding claims, characterized in that it comprises a supplemental step of~~ claim 7, further comprising reducing the thickness of said superstrate ~~(3)~~ and/or substrate.

20. (Currently amended): The application of the method as claimed in ~~any one of the preceding claims~~ claim 7 to the fabrication of silicon on insulator (S.O.I.) plates for the fabrication of integrated electronic circuits and/or integrated opto-electronic circuits.

21. (Currently amended): A structure in the form of a plate comprising at least one substrate ~~(2)~~, a superstrate ~~(3)~~ and at least one intermediate layer ~~(4)~~ interposed between the substrate and the superstrate, ~~characterized in that said~~wherein the intermediate layer ~~(4)~~ comprises at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material so that, under the effect of a heat treatment, the intermediate layer ~~(4)~~ becomes plastically deformable and the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities ~~(7)~~ in the intermediate layer ~~(4)~~.

22. (Currently amended): The structure as claimed in claim 21, ~~characterized in that~~ wherein the substrate ~~(2)~~ and the superstrate ~~(3)~~ are formed from monocrystalline silicon and the intermediate layer ~~(4)~~ is formed from doped silica.

23. (Currently amended): The structure as claimed in ~~either of claims 21 and 22, characterized in that~~ claim 21, wherein the base material is silica and the extrinsic atoms are atoms of phosphorus or boron, thus forming an intermediate layer of phospho-silicate glass (P.S.G.) or boro-phospho-silicate glass (B.P.S.G.).

24. (Currently amended): The structure as claimed in claim 23, ~~characterized in that~~ wherein the concentration of phosphorus is in the range from 8% to 14%.

25. (Currently amended): The structure as claimed in claim 23, ~~characterized in that~~ wherein the concentration of boron is in the range from 0% to 4%.

26. (Currently amended): The structure as claimed in ~~any one of claims 21 to 25, characterized in that~~ claim 21, wherein the substrate and/or the superstrate have portions ~~(8)~~ projecting into said intermediate layer ~~(4)~~.

27. (Currently amended): The structure as claimed in claim 26, ~~characterized in that~~ wherein the projecting portions ~~(8)~~ are rectilinear and extend to the sides.

28. (Currently amended): The structure as claimed in ~~any one of claims 21 to 27, characterized in that~~ claim 21, wherein at least some of said micro-bubbles or micro-cavities ~~(7)~~ are open-celled and at least some thereof constitute channels.

29. (New): The method as claimed in claim 1, further comprising producing projecting portions in the substrate and/or the superstrate on said intermediate layer side.

30. (New): The method as claimed in claim 29, wherein the projecting portions are rectilinear and extend to the sides of the intermediate layer.

31. (New): The method as claimed in claim 1, wherein at least some of said micro-bubbles or micro-cavities are open-celled and at least some thereof constitute channels.

32. (New): The method as claimed in claim 1, further comprising reducing the thickness of said superstrate and/or substrate.

33. (New): The application of the method as claimed in claim 1 to the fabrication of silicon on insulator (S.O.I.) plates for the fabrication of integrated electronic circuits and/or integrated opto-electronic circuits.